On the Performance of Low-Noise Low-DC-Power-Consumption Cryogenic Amplifiers

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***Abstract*—The performance of broad-band low-noise low-dc-power-consumption cryogenic amplifiers have been studied in detail with emphasis on minimizing the power consumption and optimizing the amplifier performance at cryogenic temperature. A general approach is presented for the modeling and amplifier design, which helps in minimizing the power consumption and optimizing the performance of the amplifier. A noise temperature below 9 K and 22-dB gain was experimentally obtained in the frequency range of 4–8 GHz with a total power consumption of 4 mW with commercial GaAs transistors.**

***Index Terms*—Empirical large-signal models, FET, FET noise models, modeling, noise model extraction, noise parameter.**

I. Introduction

InP TRANSISTOR devices are known for their very good noise performance and low dc power consumption [1]–[5]. In recent years, the performance of microwave GaAs and InP transistors has improved significantly and many successful designs with high performance have been reported [1]–[5]. GaAs devices have also obtained improved performance and especially the metamorphic InAlAsGaAs on GaAs substrate have improved very much [6].

This, together with the existence of simple and accurate models [7]–[13], has improved the quality of microwave cryogenic amplifiers and excellent results have been achieved in recent years. For many different applications, such as deep space communication, a low-dc-power dissipation can be a crucial requirement for the system.

II. Device Modeling

From on-wafer measurements of dc S-parameter and noise measurements both at room and cryogenic temperatures, noise models parameters [7]–[14] were extracted and subsequently used for the amplifier design. The transconductance of both InP and GaAs transistors increases at low temperatures (Figs. 1 and 2). Thus, a very high transconductance can be obtained at low drain voltages and low dissipated power (Fig. 3). As can be seen

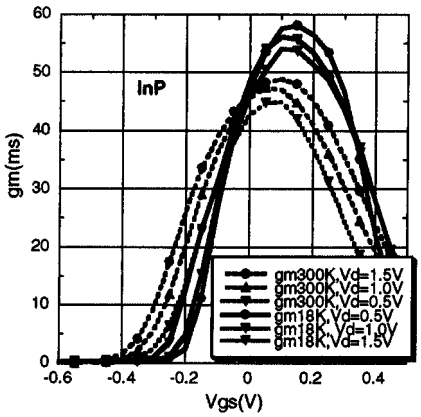

Fig. 1. g_m versus $P_{\rm dc}$ for InP transistor.

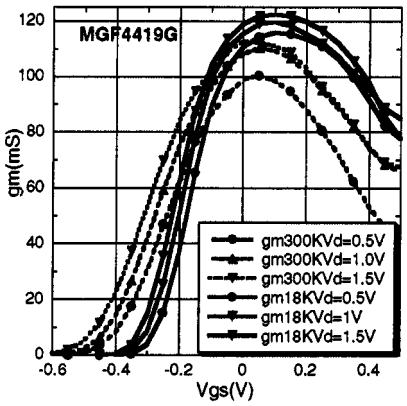

Fig. 2. g_m versus $P_{\rm dc}$ for GaAs FET MGF4419G.

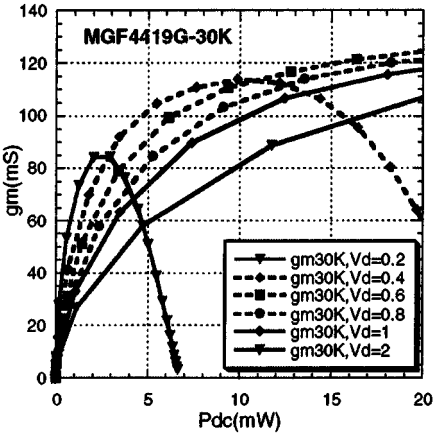

Fig. 3. g_m versus $P_{\rm dc}$ for GaAs FET MGF4419G.

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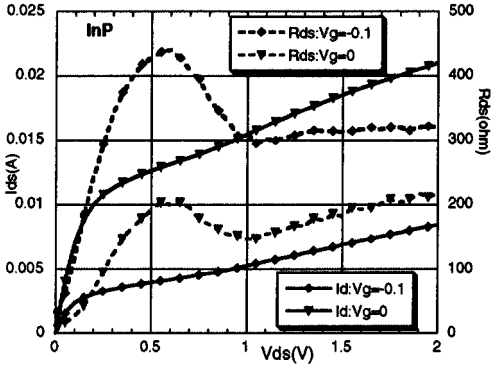

Fig. 4. $I_{\rm ds}, R_{\rm ds}$ for InP transistor.

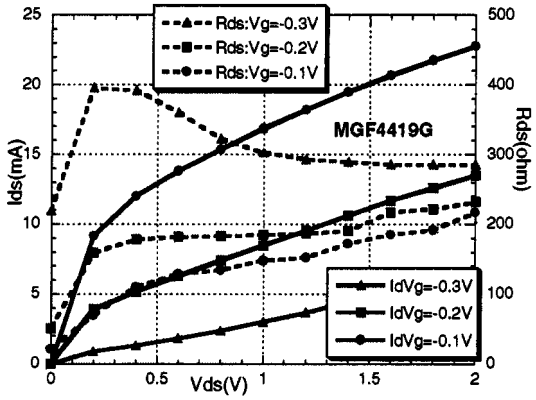

Fig. 5. $I_{\rm ds}, R_{\rm ds}$ for MGF4419G.

in Fig. 3, high transconductance can be reached with 2–3-mW dissipated dc power and a drain voltage below $V_{\rm ds} = 0.8$ V.

At very low drain voltages, $V_{\rm ds} < 0.3$–0.4 V, the output conductance is rather high and this can produce a significant reduction of transistor gain (Figs. 4 and 5). Also, at very low $V_{\rm ds}$, almost all other transistor parameters, i.e., $C_{\rm gs}, C_{\rm gd}, g_m f_t, \ldots,$ vary significantly.

Fig. 6 shows the measured S_{11}, S_{22}, and $\Gamma_{\rm opt}$ for GaAs transistor MGF4419G (Mitsubishi). From the imaginary part of Y_{11} and Y_{12} (Figs. 7 and 8), it can be seen that the capacitive part of the transistor changes significantly at drain voltages $V_{\rm ds}$ below 0.4 V.

This situation is similar for InP high electron mobility transistors (HEMTs) and can create problems in the design of broad-band amplifiers because of the large change upon bias $(V_{\rm ds})$ of the transistor parameters Y_{11}, Y_{12}, g_m, f_t and the respective sensitivity of amplifier performance.

Fig. 9 shows the equivalent circuit of the transistor and the main parameters are listed in Tables I–III. The transconductance $g_m, C_{\rm gs}, C_{\rm gd}$, and $R_{\rm ds}$ depend strongly on $V_{\rm ds}$ and the conventional simplified (1) for f_t will predict f_t with significant error. We have found (2) to be more accurate [15] as follows:

$$f_t = \frac{g_m}{2\pi\left(C_{\rm gs} + C_{\rm gd}\right)} \tag{1}$$

$$f_t = \frac{g_m}{2\pi\left[C_{\rm gs} + C_{\rm gd}\right]} \cdot \frac{1}{\left[1 + (R_s + R_d)/R_{\rm ds}\right] + C_{\rm gd} \cdot g_m \cdot (R_s + R_d)} \tag{2}$$

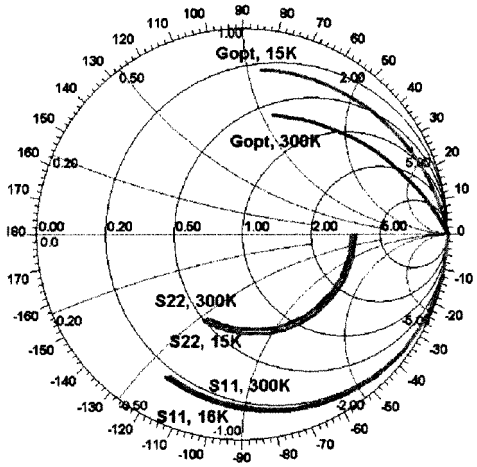

Fig. 6. S_{11} and $G_{\rm opt}$ at 15and 300 K for MGF4419G.

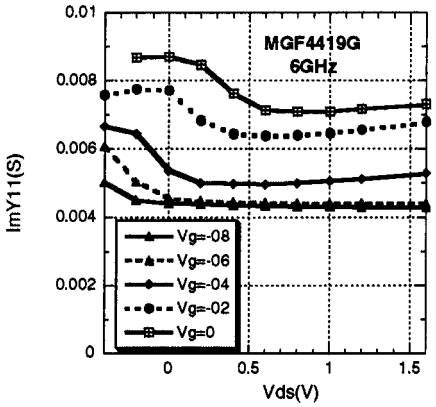

Fig. 7. $\mathrm{Im}(Y_{11})$ for MGF4419G, $f = 6$ GHz, $I_{\rm ds} = 5$ mA.

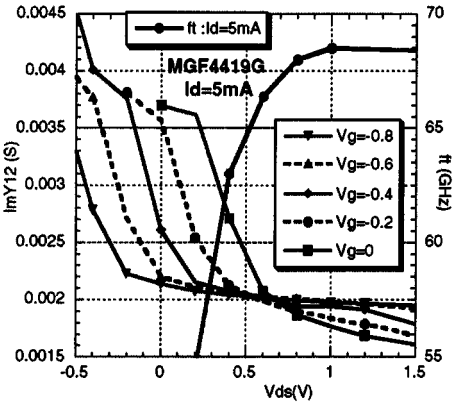

Fig. 8. $\mathrm{Im}(Y_{12})$, f_t for MGF4419G, $f = 6$ GHz, $I_{\rm ds} = 5$ mA.

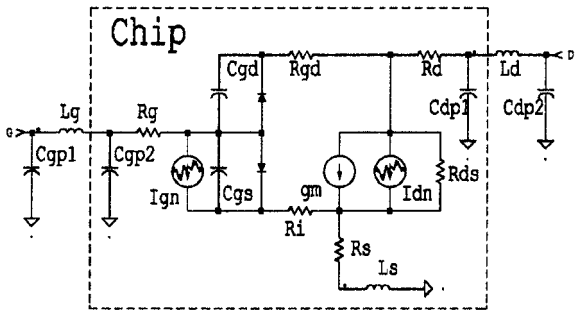

Fig. 9. Equivalent circuit of the transistor.

TABLE I
MGF4419G, 8 GHz

Vds=0.4 Id=10mA	g_m mS	g_d mS	T_m K	Z_{opt} Ω	R_n Ω	T_d K	R_i Ω
T=300K	89.4	12	35	50+j101	15.2	2100	2
T=15K Id=5mA	83.6	9	4.5	20+j100	3.85	870	1.9
Vds=1V Id=10mA	g_m mS	g_d mS	T_m K	Z_{opt} Ω	R_n Ω	T_d K	R_i Ω
T=300K	89.0	7.4	30	57+j105	12.8	2750	1.8
T=15K Id=5mA	85.8	6.4	3.7	23+j104	3.1	1000	1.8

TABLE II

I_{pk0}	P_1	P_2	P_3	V_{pks}	DV_{ps}	α_r	α_s	λ	B_1	B_2
56	2.2	-0.3	2.2	0.15	0.25	0.1	2.5	0.22	0.7	3.2

C_{gs0}	P_{10}	P_{11}	P_{20}	P_{21}	C_{gd0}	P_{30}	P_{31}	P_{40}	P_{41}	C_{gdp}
42	0	1.8	0	0.3	42	0	0.3	0	1.8	15

TABLE III

t_m	K_{nd1}	K_{nd2}	K_{ng1}
5	15.1	0.4	120

where

$$g_m = I_{\rm pk} P_1 \cdot \sec h\big(P_1.V_{\rm gs}\big)^2 \tanh(\alpha V_{\rm ds})(1+\lambda V_{\rm ds}) \quad (3)$$

$$g_{\rm ds} = I_{\rm pk}\big(1+\tanh(\psi)\big)\big(\alpha(1+\lambda V_{\rm ds})\sec h(\alpha\cdot V_{\rm ds})^2 + \lambda\tanh(\alpha V_{\rm ds})\big) \quad (4)$$

$$C_{\rm gs} = C_{\rm gsp} + C_{\rm gs0}\big(1+\tanh[P_{10}+P_{11}\cdot V_{\rm gs}]\big) \cdot \big(1+\tanh[P_{20}+P_{21}\cdot V_{\rm ds}]\big) \quad (5)$$

$$C_{\rm gd} = C_{\rm gdp} + C_{\rm gd0}\big(1+\tanh[P_{30}-P_{31}\cdot V_{\rm ds}]\big) \cdot \big(1+\tanh[P_{40}+P_{41}\cdot V_{\rm gd}]\big) \quad (6)$$

$$I_{\rm ds} = I_{\rm pko}\cdot\big(1+\tanh(\psi)\big)\tanh(\alpha V_{\rm ds})(1+\lambda V_{\rm ds}). \quad (7)$$

For details concerning this model, see [21] and [22]. As the drain voltage increases above $V_{\rm ds} > 0.5$ V, the total gate capacitance is nearly constant (Y_{11}) (Fig. 7), Y_{12} $(C_{\rm gd})$ does not change significantly (Fig. 8), and the intrinsic f_t follows the g_m dependence and is reaching a maximum at a drain voltage approximately equal to the knee voltage (where the drain voltage is just sufficient to saturate the carrier velocity). In order to simultaneously optimize the noise performance and minimize the dc power consumption, the noise models computed from the large-signal model can be used. This can also help to optimize device size for the desired frequency of operation because all parameters needed to calculate the noise parameters and dissipated power are available from the noise and large-signal transistor models [7]–[14], [21], [22].

The dc and S measurements that are required to extract the small- and large-signal equivalent circuit were supplemented with 50-Ω noise measurements [16] (Fig. 10). The main linear, nonlinear, and noise model parameters were extracted from

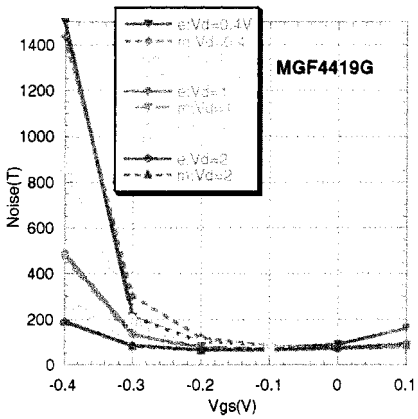

Fig. 10. Noise temperature for MGF4419G at 5 GHz. $G = 50\ \Omega$, 300 K. m: model. e: experimental.

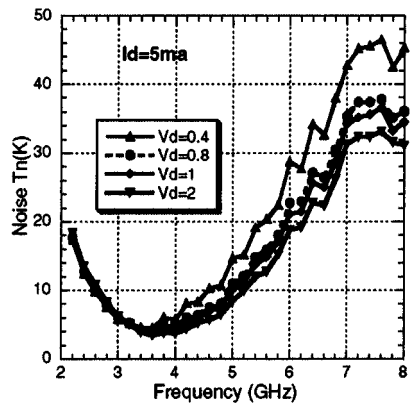

Fig. 11. Noise temperature for MGF4419G at 18 K. $I_{\rm ds} = 5$ mA.

these measurements. This approach is particularly useful in cryogenic noise model extraction.

In order to precisely evaluate the noise model, a special pre-matched circuit was designed. This is required since the noise temperature, which can be obtained from the high-quality low-noise transistors both at room and at cryogenic temperatures, is very low [2–5 K (see Fig. 11)], which is of the order of the accuracy of a conventional noise measurement system. It is also difficult to use tuners at cryogenic temperatures and, in addition, the designer can face stability problem since high-quality GaAs and InP transistors have very high gain when cooled. The use of the pre-matching circuit solves many of these problems.

Using measured transistor S-parameters and noise parameters and taking into account the bias networks required to stabilize the transistor at cryogenic temperatures, a simple input matching network is designed for the center frequency of interest. The transistor is bonded into the fixture. The bonding inductance, together with the input matching network, resonate the transistor at the center frequency of the pre-match circuit. In the study, we used GaAs chip transistors MGF4419G and different InP transistors. The gain from the single transistor is typically 10–14 dB, which is why in order to improve the overall accuracy of the noise measurements, a 26-dB room-temperature low-noise amplifier is used to minimize the noise contribution of the system. Both the hot–cold load and cold attenuator method were used for the noise measurements, and the accuracy of the noise measurements is believed to be of the order

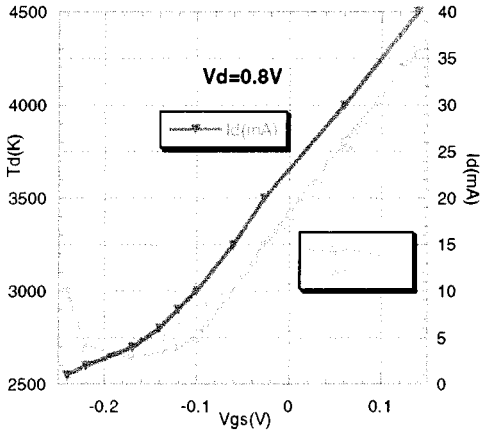

Fig. 12. T_d versus $V_{\rm gs}$ for MGF4419G at 18 K. $V_{\rm ds} = 0.8$ V.

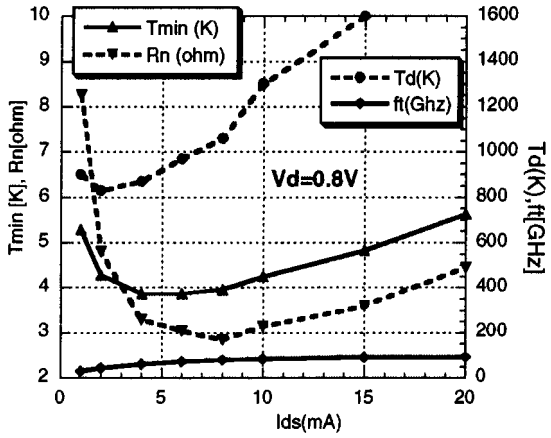

Fig. 13. $T_{\rm min}, R_n, T_d, F_t$ versus $I_{\rm ds}$ for MGF4419G at 18 K.

of 1 K. The accuracy of the noise measurements was evaluated by measuring the amplifiers at the Jet Propulsion Laboratory (JPL), Pasadena, CA, the National Radio Astronomy Observatory (NRAO), Charlottesville, VA, and Centro Astronomico de Yebes, Yebes, Spain. All were found to be similar within 1 K.

As shown in Figs. 12–14, T_d follows the $I_{\rm ds}$ dependence on $V_{\rm ds}$ and $V_{\rm gs}$ and, thus, the same type of dependencies as those describing the $I_{\rm ds}$ can be used to describe the T_d dependence [3], [7]. This allows us to use the coefficients extracted for the large-signal current model in the T_d model (Table II) and only fit one more parameter, i.e., t_m, for the noise part as follows:

$$T_d = T_{\rm amb}\Big(1+t_m\cdot\big(1+\tanh(\psi)\tanh(\alpha V_{\rm ds})(1+\lambda V_{\rm ds})\big)\Big). \tag{8}$$

At the gate voltage for which the transconductance is at maximum, $\psi = 0$, and for $V_{\rm ds} = 0.6$–0.7 V, for which $\tanh(\alpha Vds) \approx 1$ [21], f_t is maximum. T_d is then equal to

$$T_d \approx T_{\rm amb}(1+t_m). \tag{9}$$

The noise model defined in this way [see (4)–(9)] is, in fact, a large-signal representation of the Pospieszalski noise model. The basic idea in the model [7] is that the channel resistance of the transistors is producing noise as a resistance $R_{\rm ds}$, working

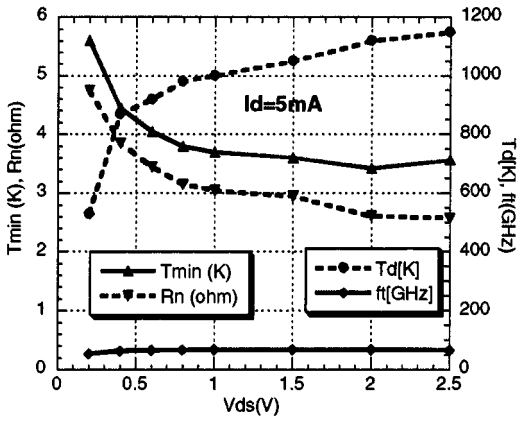

Fig. 14. $T_{\rm min}, R_n, T_d, F_t$ versus $V_{\rm ds}$ for MGF4419G at 18 K.

at temperature T_d, which is higher than the ambient temperature $T_{\rm amb}$. We have

$$R_{\rm ds} = 1/g_{\rm ds} = 1/I_{\rm pk}\big(1+\tanh(\Psi)\big)\big(\alpha(1+\lambda V_{\rm ds})\cdot\operatorname{sech}(V_{\rm ds})^2 +\lambda V_{\rm ds}\tanh(\alpha V_{\rm ds})\big). \tag{4a}$$

It has been found from many experimental investigations that the Pospieszalski noise model is very accurate [3], [4], [6], [8], [14], [19],[23] and that there is nearly linear dependence of T_d versus drain current. Fig. 12 shows measured and modeled T_d and the fit is good.

In many circuit applications and particularly in the design of cryogenic amplifiers, when good quality transistors biased for low-noise performance are used, the equivalent gate temperature T_g can be considered equal to the ambient temperature $T_g = T_{\rm amb}$. If a global model is required, T_g can be modeled using (10) since the main effect of the drain current on T_g is the heating effect

$$T_g = T_{\rm amb}\Big(1+\big(1+\tanh(\psi)\big)\tanh(\alpha\cdot V_{\rm ds})(1+\lambda\cdot V_{\rm ds})\Big). \tag{10}$$

For better accuracy, the model can be calibrated at $I_{\rm ds} = 3 \rightarrow 5$ mA (additional bias points). This means that a global model can be obtained with 2–3 noise measurements. When model parameters are available, it is possible to optimize the amplifier according to the specifications for noise, gain, and power dissipation

$$T_{\rm min} = 2\frac{f}{f_t}\sqrt{g_{\rm ds}\cdot T_d\cdot r_{\rm gs}\cdot T_g} \tag{11}$$

$$R_{\rm opt} \approx \frac{f_t}{f}\sqrt{\frac{r_{\rm gs}T_g}{g_{\rm ds}T_d}}. \tag{12}$$

In some harmonic-balance simulators, the default noise model is the Pucel, Cappy [7]–[10] three-parameter P, R, C model. When T_d and T_g are available parameters P, R, and C can be found as

$$R = g_m R_i\frac{T_g}{T_{\rm amb}} \quad P = \frac{g_{\rm ds}}{g_m}\frac{T_d}{T_{\rm amb}} + R \quad C = \sqrt{\frac{R}{P}}. \tag{13}$$

This will work well with saturated drain voltages, but when $V_{\rm ds}=0$ and $g_m=0$, the singularity in (13) in every large-signal model can cause convergence problem. This can become significant in the analysis of circuits operating at low drain voltages such as resistive, drain mixers, switches, and other circuits operating at low drain voltages. The problem can be solved by adding a small quantity to the denominator that reflects the finite output resistance of the FET or by replacing the function $1/\tanh$ with

$$1/\tanh|\alpha V_{\rm ds}| \approx 1/\left(\tanh|\alpha V_{\rm ds}|+10^{-7}\right) \approx 1+\alpha^2/\cosh|\alpha V_{\rm ds}|^2. \quad (14)$$

It is convenient to implement the noise models in the simulator using noise current sources. In the MESFET and HEMTs, the main contributor to the noise is the drain current, but, in fact, this noise is higher than the pure Johnson noise generated by $I_{\rm ds}$, and this should be accounted for. The total output current contributing to the noise is

$$I_{\rm dtn}=|I_{\rm ds}|+|I_{\rm gd}|. \quad (15)$$

The noise current generators connected at the input and output, as in Fig. 9, are

$$I_{\rm dn}=4kT\left(w\cdot 10^{-2}\right)\sqrt{K_{\rm nd1}I_{\rm dtn}+K_{\rm nd2}I_{\rm dtn}^2}$$
$$I_{\rm gn}=4kT\left(I_g+I_{\rm dtn}/K_{\rm ng1}\right)\cdot\left(2w\cdot 10^{-2}\right) \quad (16)$$

where $K_{\rm ng1}, K_{\rm nd1}$ and $K_{\rm nd2}$ are fitting coefficients and w is the device size in millimeters. If higher accuracy is required, the correlation between the noise sources can be considered. For GaAs transistor MGF4419G, these coefficients are shown in Table III.

The coefficient $K_{\rm nd1}$ describes the linear dependence between the drain current and noise, and $K_{\rm nd2}$ describes the sharp increase of the noise at high drain currents.

The model was implemented as a user-defined model in MDS-HP. As shown in Fig. 10, a high accuracy of the model can be obtained using (16). When it is not necessary to have a global model, the extraction of $K_{\rm nd2}$ can be omitted. Further, the accuracy of the global model can be improved by using the mixed empirical-table-based approach storing the $I_{\rm dtn}$ as table data [22].

When all necessary parameters for modeling the transistor are available, it is possible to optimize the amplifier according to our specific requirements concerning noise, gain, power dissipation, etc. Figs. 13, 14, and Table I show typical results for the main noise parameters and their bias dependence, obtained using the pre-matched fixture with MGF4419G. The noise temperature reaches minimum at a drain current $I_{\rm ds}=4$–5 mA. The minimum noise resistance R_n is lower at higher drain voltages because of the influence of capacitances $C_{\rm gs}, C_{\rm gd}$. Nevertheless, even at drain voltages $V_{\rm ds}=0.5$–0.7 V, a $T_{\rm min}$ below 5 K can be achieved with dissipated power of 2–3 mW per transistor. The f_t does not change much for drain voltages above $V_{\rm ds}>0.5$ V and the drain temperature T_d increase as the drain current and drain voltage increase. By using this information, it is possible to correct the noise models, design the cryogenic amplifier more precisely, and optimize the power dissipation and noise performance. Another issue is selecting the right device size to obtain optimum input capacitance $C_{\rm gs}$, high f_t, and low R_n, thus making the matching networks simple in order to achieve broad-band operation [12], [13]. These relations between $I_{\rm ds}$, dissipated power, and noise parameters are general for all FETs. It is possible to operate the transistor at drain voltages as low as $V_{\rm ds}=0.5$–0.7 V (and even lower), minimize the power consumption, and still have rather high f_t, which is one of the key parameters influencing minimum noise [7]. If this approach of combining the large-signal model with the noise model is followed, it is not necessary to make a special bias-dependent noise model, which is difficult and time consuming, especially at cryogenic temperatures. In many circuit simulators, the noise models are already associated with the large-signal models and it is sufficient to calibrate the noise part of the model at a few bias points. Today, procedures for extracting the noise models are well established, and methods used to extract parameters for the Pospieszalski noise model [14] can be used directly for extraction of the noise parameters [see (8), (11), and (12)].

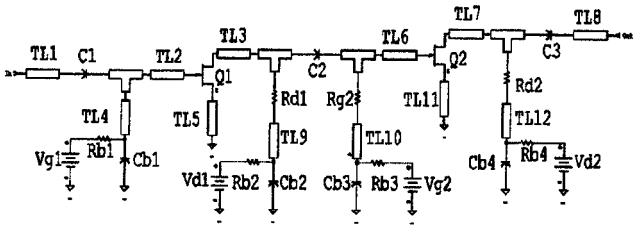

Fig. 15. Two-stage amplifier schematic.

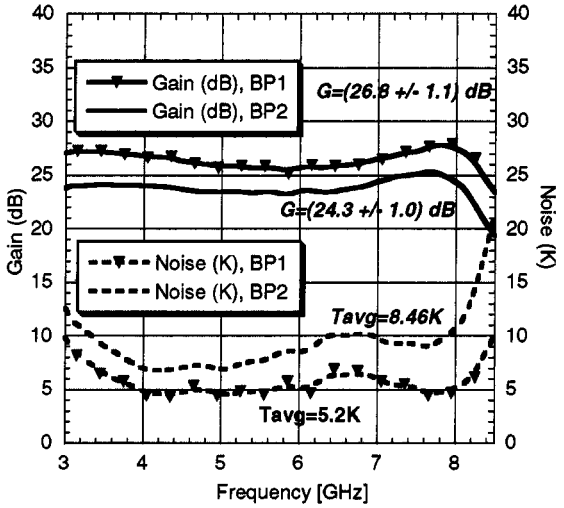

Fig. 16. Gain and noise of the amplifier at 18 K. $\rm BP_1: V_{d1}=2.2$ V, $V_{d2}=2$ V, $P_{\rm dc}=10.5$ mW/stage. $\rm BP_2: V_{d1}=0.7$ V, $V_{d2}=0.6$ V, $P_{\rm dc}=2.1$ mW/stage.

III. Amplifier Design

The amplifier structure is shown in Fig. 15. In order to improve the input match and stability, and to facilitate noise matching, an inductive source feedback was created by the bond wires. The amplifier performance is shown in Fig. 16. A gain of 22–24 dB and a noise temperature of 7–9.5 K were measured in the frequency range of 4–8 GHz with total power dissipation of 4 mW with commercial transistors. Better results can be achieved using transistors with higher f_t [6].

IV. Conclusion

The performance of low-noise transistors was studied at room and cryogenic temperatures with emphasis on minimizing the power consumption and optimizing the amplifier performance. Combining the noise model with the large-signal model can help in the design of low-noise amplifiers with minimum power dissipation. A noise temperature below 9 K and 22-dB gain (two stages) was experimentally obtained with total dc power $P_{\rm dc} = 4\,\text{mW}$ using GaAs transistors. This is close to the best-reported results with InP transistors. The noise model can also be used to design nonlinear circuits like mixers.

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